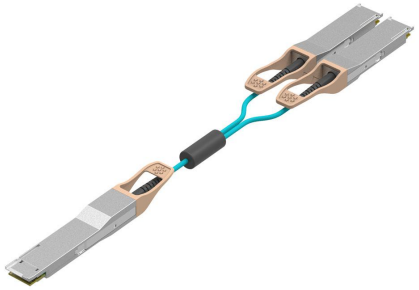
200G QSFP-DD to 2x 100G QSFP28 Breakout Active Optical Cables

P/N: GDA-MDO201-xxxC (xxx: 001 to 100)

Features:

- ✓ Hot-pluggable QSFP-DD and QSFP28 connectors
- ✓ 8 channels full-duplex 850nm parallel active optical cable
- ✓ Transmission data rate up to 25.78Gbps per channel
- ✓ 8 channels 850nm VCSEL array and PIN photo-detector array
- ✓ Internal CDR circuits within receiver and transmitter data paths
- ✓ Supports CDR bypass via I2C controlled
- ✓ Low power consumption < 4W (QSFP-DD) < 2.5W (QSFP28)
- ✓ Length up to 70m using OM3 MMF and 100m using OM4 MMF
- ✓ I^2C management interface
- ✓ Operating case temperature range 0°C to +70°C
- ✓ 3.3V power supply voltage
- ✓ RoHS 2.0 compliant (lead free)



Applications:

- ✓ IEEE 802.3bm 100GBASE-SR4

Description:

The Gigalight 200G QSFP-DD to 2x 100G QSFP28 breakout Active Optical Cable (AOC) is a direct-attach fiber assembly with one QSFP-DD MSA compliant QSFP-DD connector and two QSFP MSA compliant QSFP28 connetors. It is suitable for short distances and offer a cost-effective solution to connect within racks and across adjacent racks.

This breakout or splitter cable operates with 8 full-duplex lanes and each lane is capable of transmitting data rate at 25.78Gb/s, providing an aggregated rate of 206Gb/s. The length is up to 70 meters using OM3 MMF and 100 meters using OM4 MMF..

Module Block Diagram

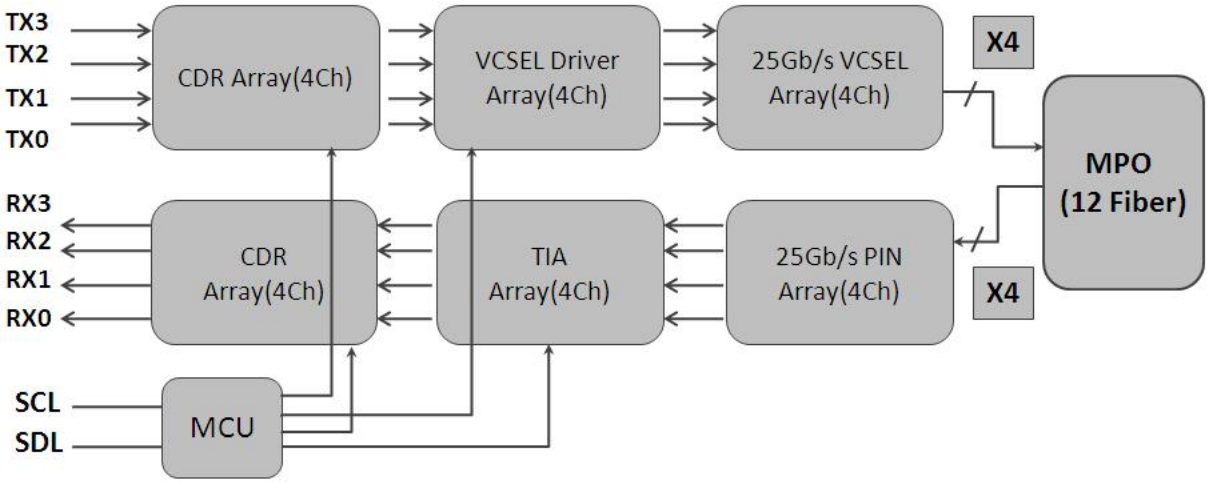


Figure 1. 100G QSFP28 SR4 Module Block Diagram

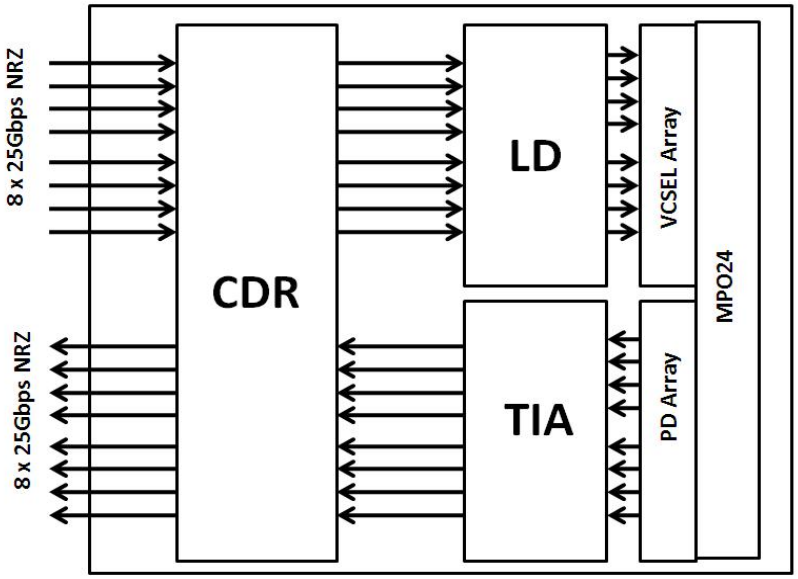


Figure 2. 200G QSFP DD Module Block Diagram

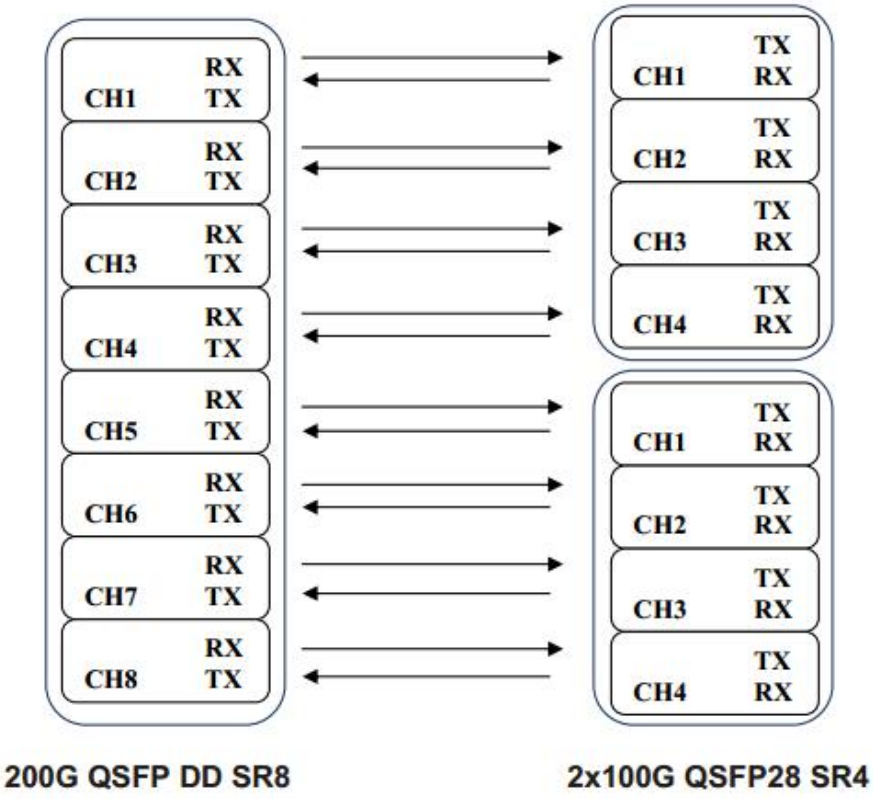


Figure 3. **AOC Block Diagram**

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane	fd		25.78125		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm		2	2.5	W
Fiber Bend Radius	Rb	3			cm

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔVin	300		1100	mVp-p
Differential output voltage amplitude	ΔVout	500		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate[1]	BER			E-12	
Input Logic Level High[2]	VIH	2.0		VCC	V
Input Logic Level Low[2]	VIL	0		0.8	V
Output Logic Level High[3]	VOH	VCC-0.5		VCC	V
Output Logic Level Low[3]	VOL	0		0.4	V

Note:

1. BER=10^-12; PRBS 2^31-1@25.78125Gbps.
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	840	850	860	nm	-
RMS spectral width	Δλ	-	-	0.6	nm	-
Average launch power, each lane	Pout	-8.4	-	2.4	dBm	-
Optical Modulation Amplitude (OMA),each lane	OMA	-6.4		3	dBm	-
Transmitter and dispersion eye closure(TDEC),each lane	TDEC			4.3	dB	
Extinction Ratio	ER	3	-	-	dB	-
Average launch power of OFF transmitter, each lane				-30	dB	-
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	SPECIFICATION VALUES {0.3,0.38,0.45,0.35,0.41.0.5}					Hit Ratio = 5x10-5
Receiver						
Centre Wavelength	λc	840	850	860	nm	-
Stressed receiver sensitivity in OMA				-5.2	dBm	1
Maximum Average power at receiver , each lane input, each lane				2.4	dBm	-
Minimum Average power at				-10.3	dBm	

receiver , each lane						
Receiver Reflectance				-12	dB	-
LOS Assert		-30			dBm	-
LOS De-Assert – OMA				-7.5	dBm	-
LOS Hysteresis		0.5			dB	-

Pin Descriptions (100G QSFP28 SR4)

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I /O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	

34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

Notes:
1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand 3.6V.

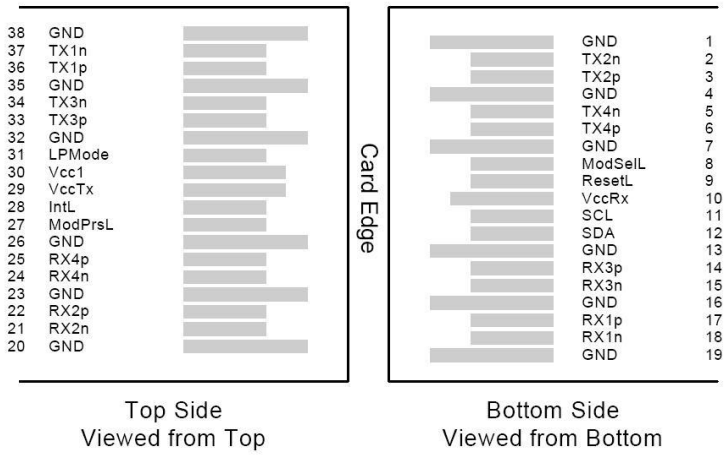


Figure 4. Electrical Pin-out Details

ModSelL Pin
The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin
Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin
Gigalight QSFP28 SR4 operate in the low power mode (less than 1.5 W power consumption)
This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin
IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering (100G QSFP28 SR4)

The host board should use the power supply filtering shown in Figure5.

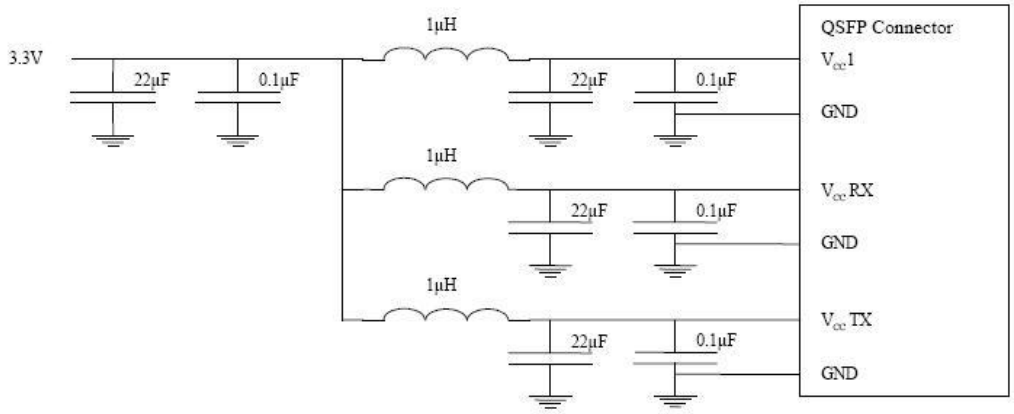


Figure 5. Host Board Power Supply Filtering

Memory Map (100G QSFP28 SR4)

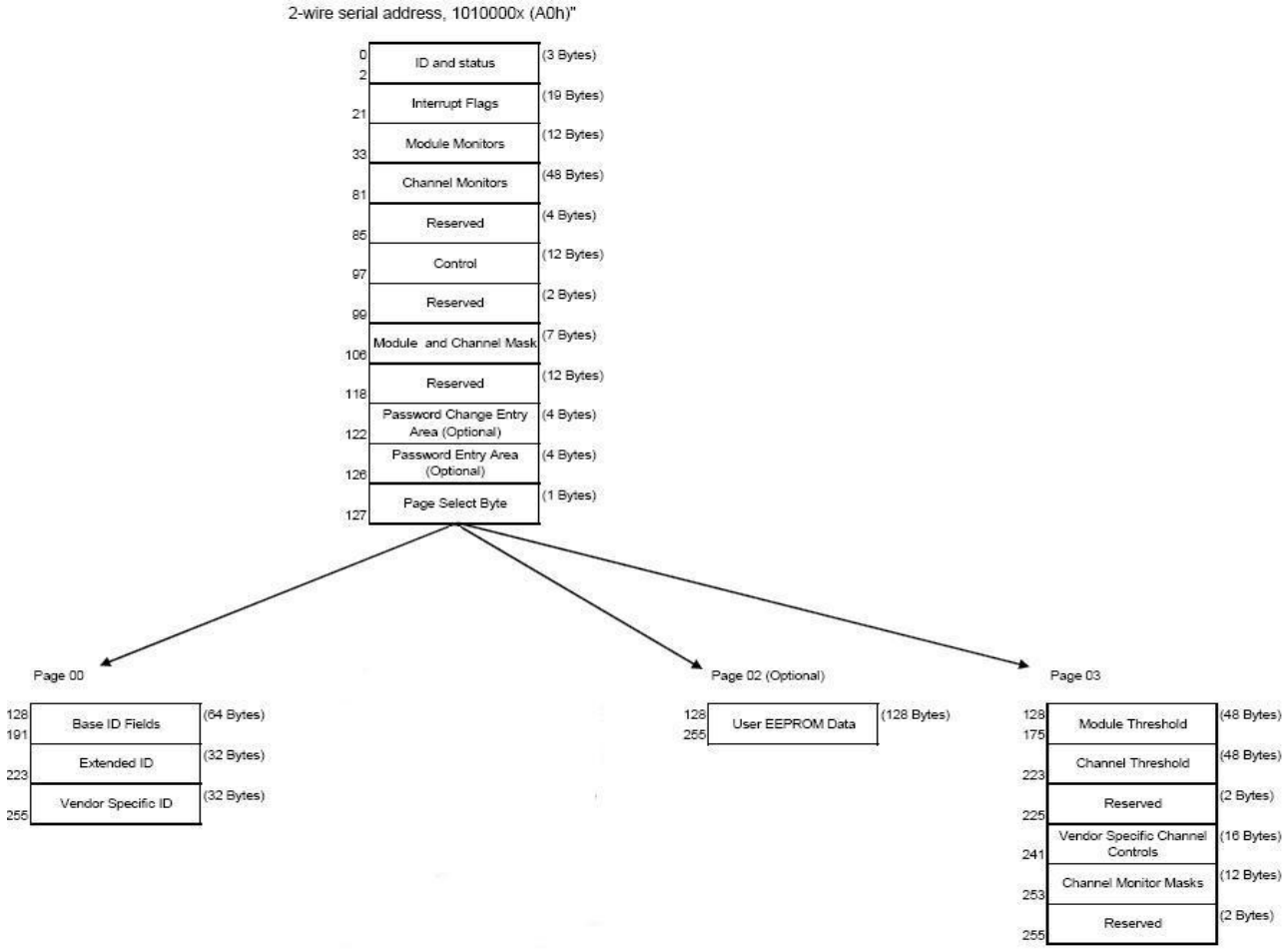


Figure5. QSFP Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure6. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure7. Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 μm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 μm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125μm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand†
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure8. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and page00.page03 upper memory please see SFF-8436 document.

Pin Description (200G QSFP DD SR8)

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground[1]
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground[1]
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground[1]
8	LVTTL-I	MODSEIL	Module Select[2]
9	LVTTL-I	ResetL	Module Reset[2]
10		VCCRx	+3.3V Receiver Power Supply
11	LVCMOS-I/O	SCL	2-wire Serial interface clock[2]
12	LVCMOS-I/O	SDA	2-wire Serial interface data[2]
13		GND	Module Ground[1]
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground[1]
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground[1]
20		GND	Module Ground[1]
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground[1]
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground[1]
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND[2]
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE[2]
32		GND	Module Ground[1]
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground[1]
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground[1]
39		GND	Module Ground[1]
40	CML-I	Tx6-	Transmitter inverted data input
41	CML-I	Tx6+	Transmitter non-inverted data input

42		GND	Module Ground[1]
43	CML-I	Tx8-	Transmitter inverted data input
44	CML-I	Tx8+	Transmitter non-inverted data input
45		GND	Module Ground[1]
46		Reserved	For future use
47		VS1	Module Vender Specific 1
48		VCCRx1	+3.3V Power Supply
49		VS2	Module Vender Specific 2
50		VS3	Module Vender Specific 3
51		GND	Module Ground[1]
52	CML-O	RX7+	Receiver non-inverted data output
53	CML-O	RX7-	Receiver inverted data output
54		GND	Module Ground[1]
55	CML-O	RX5+	Receiver non-inverted data output
56	CML-O	RX5-	Receiver inverted data output
57		GND	Module Ground[1]
58		GND	Module Ground[1]
59	CML-O	RX6-	Receiver inverted data output
60	CML-O	RX6+	Receiver non-inverted data output
61		GND	Module Ground[1]
62	CML-O	RX8-	Receiver inverted data output
63	CML-O	RX8+	Receiver non-inverted data output
64		GND	Module Ground[1]
65		NC	N0 Connect
66		Reserved	For future use
67		VCCTx1	+3.3V Power Supply
68		VCC2	+3.3V Power Supply
69		Reserved	For future use
70		GND	Module Ground[1]
71	CML-I	Tx7+	Transmitter non-inverted data input
72	CML-I	Tx7-	Transmitter inverted data input
73		GND	Module Ground[1]
74	CML-I	Tx5+	Transmitter non-inverted data input
75	CML-I	Tx5-	Transmitter inverted data input
76		GND	Module Ground[1]

Note:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

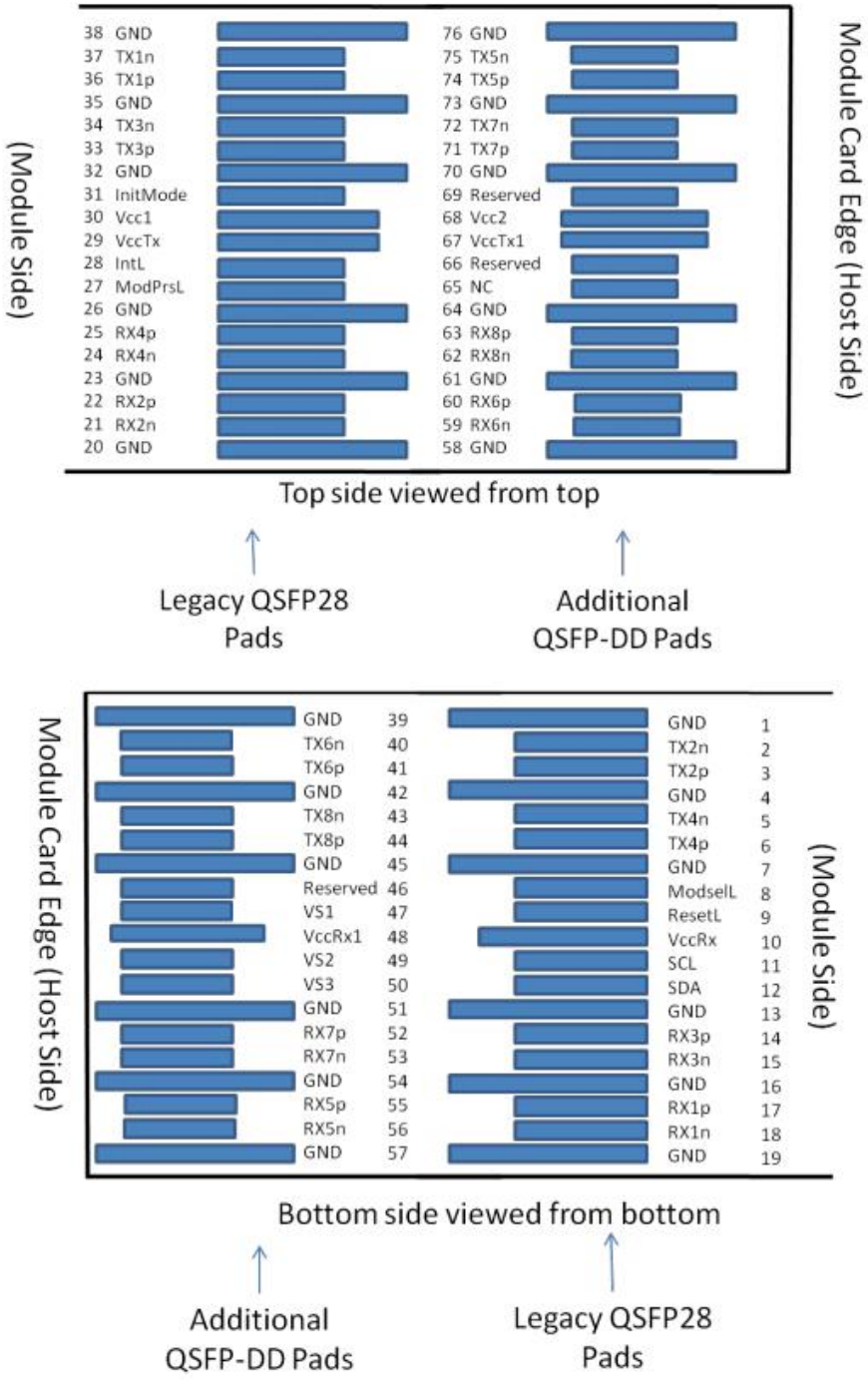


Figure 9. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

InitMode Pin

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module (see Table 2). The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP-DD Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

ModPrsL Pin

ModPrsL must be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull up resistor on the host board.

IntL Pin

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board (see Table 2). When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read..

Power Supply Filtering (200G QSFP DD SR8)

The host board should use the power supply filtering shown in Figure 10.

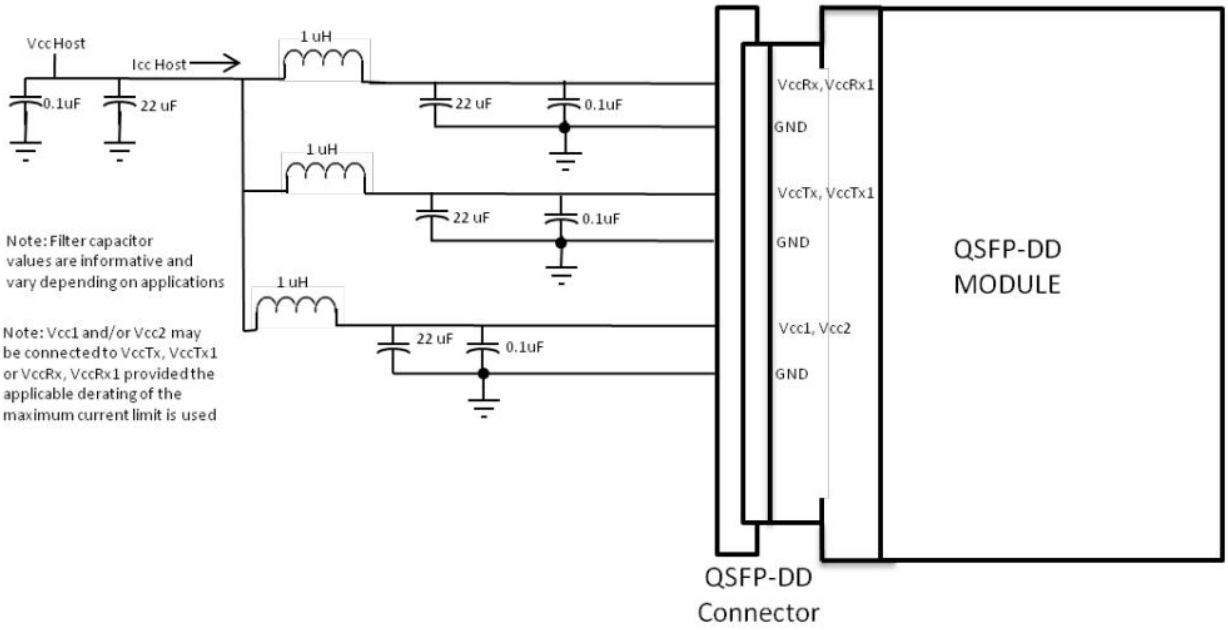


Figure 10. Host Board Power Supply Filtering

Memory Map (200G QSFP DD SR8)

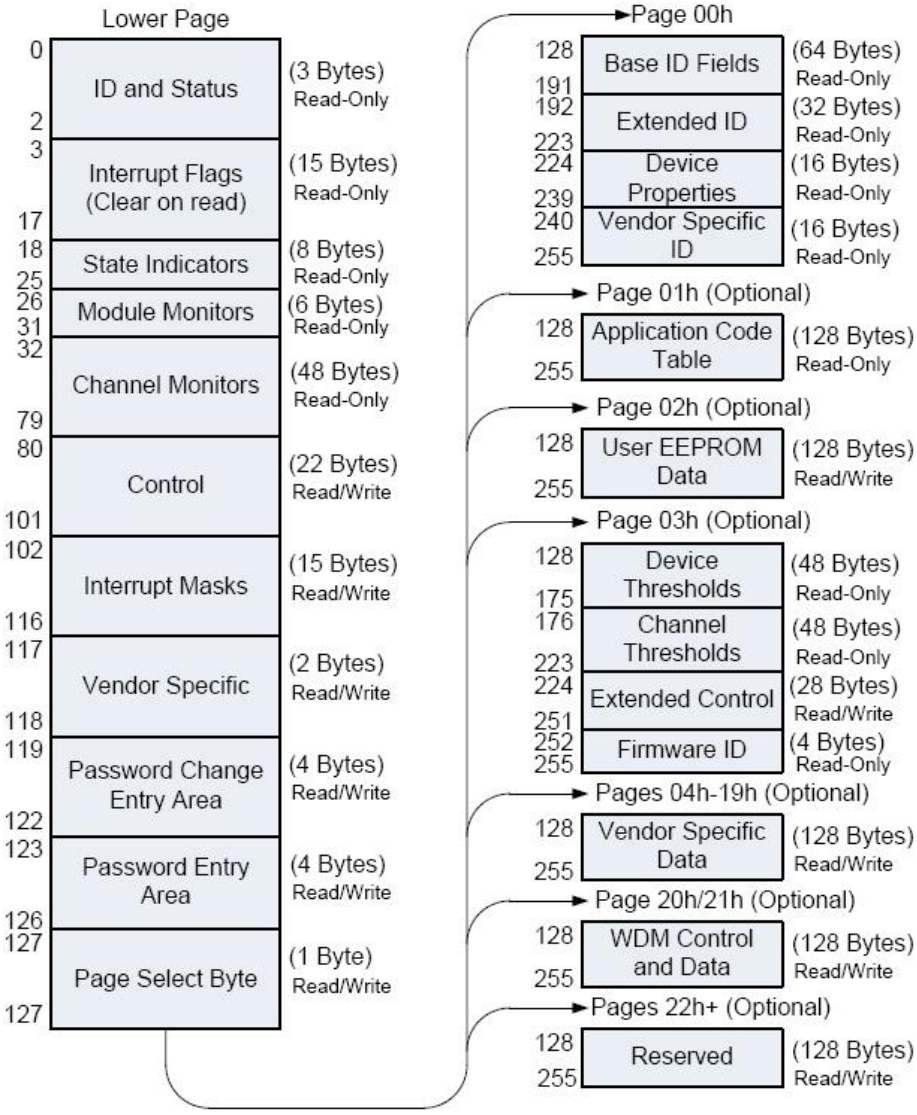


Figure 11. QSFP DD Memory Map

Table 16- Lower Page Overview (Lower Page)

Address	Description	Type
0 – 2	Id and Status (3 bytes)	Read-only
3 – 17	Interrupt Flags (15 bytes)	Read-only
18 – 25	State Indicators (8 bytes)	Read-only
26 – 31	Module card Monitors (6 bytes)	Read-only
32 – 79	Channel Monitors (48 bytes)	Read-only
80 – 101	Control Fields (22 bytes)	Read/Write
102 – 116	Interrupt Flag Masks (15 bytes)	Read/Write
117 – 118	Reserved	Read/Write
119 – 122	Password Change Area (4 bytes)	Write-Only
123 – 126	Password Entry Area (4 bytes)	Write-Only
127	Page Select Byte	Read/Write

Figure 12. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure 13. Page 03 Memory Map

Table 28- Upper Page 0 Overview (Page 00h)

Address	Size (bytes)	Name	Description
Base ID Fields:			
128	1	Identifier	Identifier Type of module
129	1	Ext. Identifier	Extended Identifier
130	1	Connector Type	Code for media connector type
131-138	8	Specification compliance	Code for electronic compatibility or optical compatibility
139	1	Encoding	Code for serial encoding algorithm
140	1	BR, nominal	Nominal bit rate, units of 100 MBits/s
141	1	Extended rate select compliance	Tags for extended rate select compliance
142-146	5	Link length	Link length / transmission media
147	1	Device technology	Device technology
148-163	16	Vendor name	Vendor name (ASCII)
164	1	Extended Module	Extended Module codes for InfiniBand
165-167	3	Vendor OUI	Vendor IEEE company ID
168-183	16	Vendor PN	Part number provided by vendor (ASCII)
184-185	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
186-187	2	Wavelength or Copper cable Attenuation	Nominal laser wavelength (wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5GHz (Adrs 186) and 5.0GHz (Adrs 187)
188-189	2	Wavelength tolerance	Guaranteed range of laser wavelength(+/- value) from nominal wavelength.(wavelength Tolerance=value/200 in nm)
190	1	Max case temp.	Maximum case temperature in degrees C
191	1	CC_BASE	Check code for base ID fields (addresses 128-190 inclusive)
Extended ID Fields:			
192-195	4	Options	Indicates which optional capabilities are implemented in the module
196-211	16	Vendor S/N	Vendor product serial number
212-219	8	Date Code	Vendor's manufacturing date code
220	1	Diagnostic Monitoring Type	Indicates which types of diagnostic monitoring are implemented in the module
221-222	2	Enhanced Options	Indicates which optional enhanced features are implemented in the module.
223	1	CC_EXT	Check code for the Extended ID Fields (addresses 192-222 inclusive)
224-238	15	Device Properties	Provides detailed information about the device
239	1	CC-PROP	Check code for the Device Properties Fields (addresses 224-2382 inclusive)
Vendor Specific ID Fields:			
240-255	16	Vendor-Specific	Vendor-specific ID information

Figure 14. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and Page 00.Page 03 upper memory please see SFF-8436 document.

Mechanical Dimensions

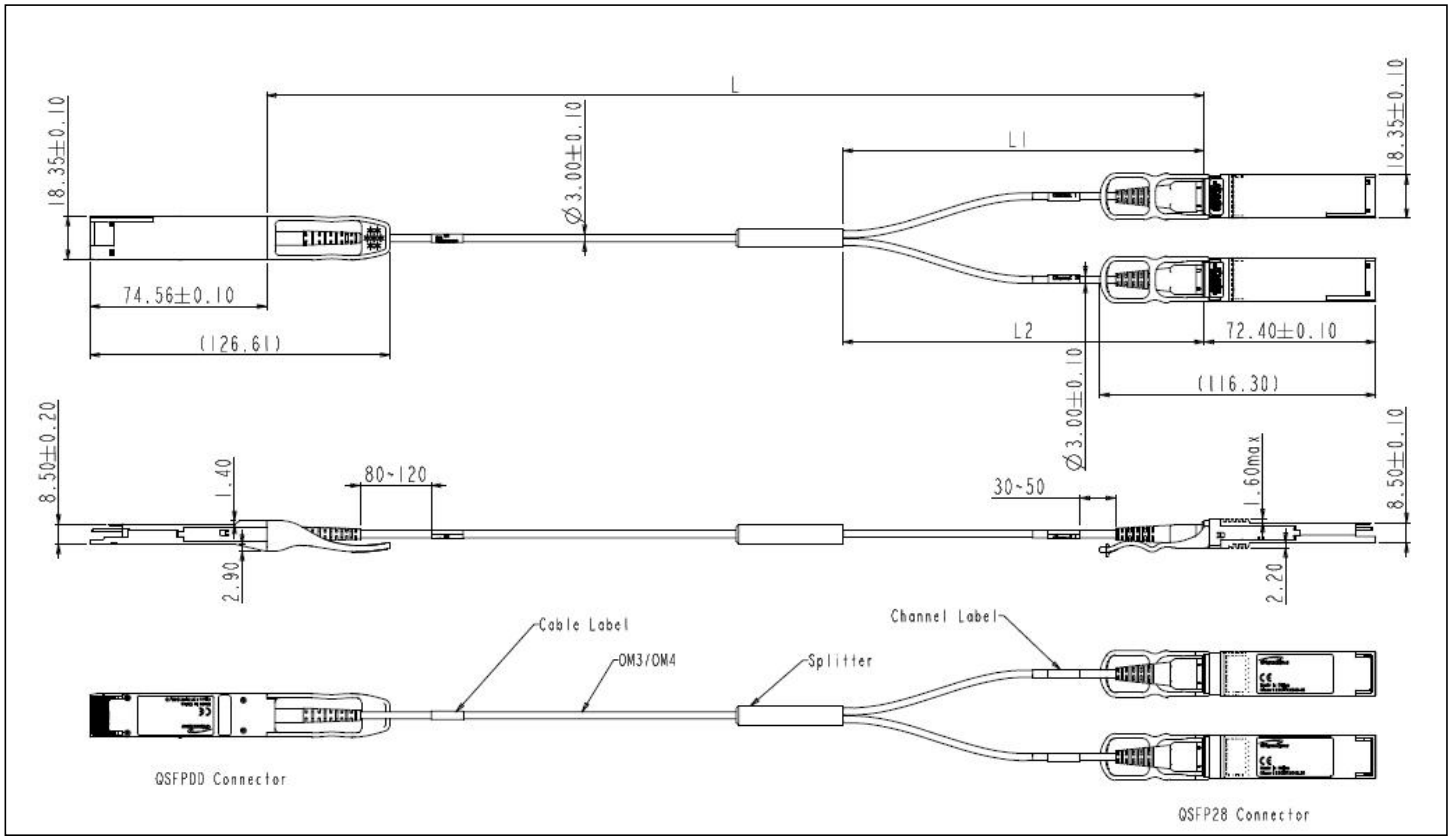


Figure 15. AOC Mechanical Specifications

Regulatory Compliance

The Gigaligth AOC cables are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50
Laser Eye Safety	TÜV	IEC 60825-1:2014 EN 60825-1:2014 EN 60825-2:2004+A1+A2
Electrical Safety	TÜV	EN 60950-1:2006+A11+A1+A12+A2
Electrical Safety	UL/CSA	UL 60950-1 & CAN/CSA C22.2 No.60950-1 CLASS 3862.07 CLASS 3862.87
EMC	FCC	47 CFR FCC Part 15 Subpart B

EMC	CE-EMC	EN 55032:2015 EN 55024:2010+A1:2015 EN 61000-3-2:2014 EN 61000-3-3:2013

Complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007.

References

1. QSFP-DD MAS Rev2.0
2. QSFP28 MSA
3. Ethernet 100GBASE-SR4 IEEE 802.3bm
4. IEEE 802.3bm, PMD Type 100GBASE-SR4.
5. Directive 2011/65/EU of the European Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment,” July 1, 2011.

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part Number	Product Description
GDA-MDO201-xxxC	200G QSFP-DD to 2x 100G QSFP28 AOC, 206Gb/s, length up to 70m (OM3 MMF) and 100m (OM4 MMF)

Important Notice

Performance figures,data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

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Revision History

Revision	Date	Description
V0	Nov-23- 2018	Advance Release.